Agenda

- Digital Terminology
- Waveform Characteristics
- Digital IO Modes
- Timing
- Eye Diagrams
- Error in DIO
- Common Applications of HSDIO
- Digital Waveform Editor
- NI HSDIO Driver
**Digital Terminology**

- **Bit** – The smallest unit of data. Each bit is either a 1 or a 0
- **Byte** – A binary number consisting of 8 related bits of data
- **Line** – One individual signal in a port. Bit refers to the data transferred. Line refers to the hardware
- **Port** – A collection of digital lines (usually 4 or 8)
- **Port Width** – Number of lines per port (usually 4 or 8)
- **Mask** – Determines which lines are read from or written to
Voltage Definitions

- Single-ended digital signals (TTL, CMOS, RS-232…)
  - $V_{OH}$
  - $V_{OL}$

- Differential digital signals (LVDS, ECL, PECL, RS-422…)
  - $V_{diff}$
  - $V_{CM}$
Waveform Characteristics

- Rise Time & Fall Time

Preshoot and Overshoot
Waveform Characteristics

• Settling Time

Duty Cycle

50% Duty Cycle

30% Duty Cycle
Digital I/O Modes

• Static I/O
  • Update or read the state of digital lines programmatically
  • Limited to slow transfers

• Handshaking
  • Each device alerts the other when conditions are met
  • Handshaking protocol specifies when, how and why one or more handshaking lines are controlled
  • Good protection against bit errors
Digital I/O Modes (Continued)

Change Detection
- Device detects when the state of each line changes
- Susceptible to noise

Dynamic I/O (a.k.a. Strobed I/O or Pattern I/O)
- Data is updated and read in relation to a separate clock signal
- Good mechanism for rapid data transfer
- Hardware timed
- Requires a memory buffer on the digital device
- Timing considerations, such as setup and hold time apply
Timing

- Dynamic digital signals reference a clock signal
- Digital Transmitters update on the transmitting assertion edge of the clock
- Digital Receivers sample on the receiving assertion edge of the clock
- Assertion edges can be rising or falling and the transmitting edge need not be the same as the receiving
- Data lines cannot change as they are being sampled; determined by setup time and hold time
Timing

- **Setup and Hold Time**
  - Constraints on the transmitter, determined by the receiver
  - Setup time – Amount of time that data signal must be stable before the assertion edge of the sample clock
  - Hold time – Amount of time that data signal must be stable after the assertion edge of the sample clock
Eye Diagrams

- Analog representations of a digital signal
Eye Diagram
Eye Diagram

Voltage Noise

Jitter
Eye Diagram
Eye Diagram
Eye Diagram

V_{IH}

V_{IL}
Eye Diagram
Error in Digital I/O - Noise

- **Resolution**
  - Proper wiring and cabling techniques
    - Differential standards
    - Wire length and placement
    - Electrical shielding
    - Magnetic shielding
    - Configuration
      - Twisted pair
      - Coaxial
  - Software filtering ineffective on binary data
Error in Digital I/O - Termination

- When the load impedance and the characteristic impedance are not the same, $Z_0 \neq Z$
- This is similar to light reflecting back from a window.

![Diagram of source, transmission line, and load with impedance symbols](ni.com)
Incorrect Termination Causes Ringing

- Reflection causes overshoot and undershoot
- The ringing could cause extra data points to be read
Incorrect Termination Increases Settling Time

- The system must wait longer for steady state.
- This increased delay can slow down data transfer.
Termination Methods

Resistors and other components can be added to match the load impedance to the transmission line characteristic impedance.

\[ R = Z_0 - Z_S \]

\[ R = Z_0 \]

\[ C = \frac{T}{2.2R} \]
Common Measurements

• Stimulus and Response (Communication)
• Digital Transmission Quality Measurement (Bit-Error Ratio)
• Analog Measurements
  o Voltage Measurement
  o Short/Stuck at Tests
  o Diode Tests
• PMU Force/Measure (PXIe-6556)
Programmable Voltage Levels

- High and Low Generation levels
- High and Low Acquisition thresholds
- Allows custom voltage standards
- Can be used for analog measurements
  - High channel count for simple analog measurements
  - Analog tests on digital circuits without a separate device
Analog Voltage Measurement

- Measure the voltage on a digital line
- Must know range of voltage and voltage must be within device limits
  - Set acquisition voltage threshold to bottom of range
  - Steadily increase acquisition threshold and read the digital value at each iteration
  - Digital value changes from 1 to 0 when the acquisition threshold equals the voltage on the line
Short/Stuck-at Fault Detection

- **Short** – Unintended connection between two digital lines
- **Stuck-at Fault** – Digital circuit is unable to change state (stuck-at-0 or stuck-at-1)
  - Generate a high voltage on one pin and low voltage on others
  - Measure the voltage on all pins using one of the voltage measurement techniques
  - If the measured voltage on one or more pins is not equal to the expected voltage then a fault is present
  - Compare the pin voltages to determine if the fault is a short or a stuck-at fault (shorts will distribute some voltage from the high pin to one of the low pins)
Diode Tests

• Diodes are often used to protect digital circuits from voltage spikes.
• The presence of a diode can be measured with a programmable voltage device:
  o Generate a voltage lower than the diode turn-on voltage:
    - Measure the voltage on the line, the voltage should be approximately equal to the generated voltage.
  o Generate a voltage higher than the diode turn-on voltage:
    - Measure the voltage on the line, the voltage should be approximately equal to the diode turn-on voltage.
• Incorrect values for either reading indicate a problem with the diode.
Software: Vector Importing Software

NI Digital Waveform Editor
- Tool to create, edit, and import DIO vectors
- Supports VCD, ASCII, binary, CSV
- Generate waveforms on NI HSDIO directly

Support for Importing WGL / STIL
- Captures pin names and timing
- Port test vectors from other testers
- Works directly with NI HSDIO
Software: SPI/I²C/JTAG Reference Libraries

High-level building blocks for constructing protocol based waveforms
Board Architecture Overview

DFC baseboard

Clock In
PFI 0
Clock Out

PLL
Programmable Power Supplies
Pin Electronics
Timing Generator & Data Formatter
# NI High Speed Digital Offering: Features

<table>
<thead>
<tr>
<th>Form Factor</th>
<th>6535/36/37</th>
<th>6541/42</th>
<th>6544/5</th>
<th>6551/52</th>
<th>6547/48</th>
<th>6555/56</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIe / PXI</td>
<td>PCI / PXI</td>
<td>1 slot PXI</td>
<td>PCI / PXI</td>
<td>1 slot PXI</td>
<td>2 slot PXI</td>
<td></td>
</tr>
<tr>
<td>Max Speed</td>
<td>10/25/50 MHz</td>
<td>50/100 MHz</td>
<td>100/200MHz</td>
<td>50/100 MHz</td>
<td>100/200MHz</td>
<td>200 MHz</td>
</tr>
<tr>
<td>Channels</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>20</td>
<td>32 / 24 (with HWC)</td>
<td>24</td>
</tr>
<tr>
<td>TTL Voltage</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>TCLK</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Data Delay</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>HWC / CCT</td>
<td></td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Prog. Voltage</td>
<td></td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Driver/Comparator</td>
<td></td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Precision Clock</td>
<td></td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Per-pin Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Per-pin Deskew</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Per-pin PMU</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Per-pin Load</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓*</td>
<td>✓*</td>
</tr>
<tr>
<td>System SMU</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓*</td>
<td>✓*</td>
</tr>
</tbody>
</table>

*6556 Only

- **Interfacing**
- **Characterization**
Thank you!