High-Speed Digital I/O
Interfacing with Digital I/O

Design

Verification & Validation
- Characterization
  - Protocol communication
  - Parametric testing
  - DUT control
  - Limit testing
  - Stress testing
  - BERT

Production

Functional Test
- Protocol communication
- Parametric testing
- DUT control
## NI High Speed Digital Offering: Features

<table>
<thead>
<tr>
<th>Form Factor</th>
<th>PCIe / PXIe</th>
<th>PCIe / PXI</th>
<th>1 slot PXIe</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Speed</td>
<td>10/25/50 MHz</td>
<td>50/100 MHz</td>
<td>100/200 MHz</td>
</tr>
<tr>
<td>Channels</td>
<td>32</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>TTL Voltage</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>TCLK</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Data Delay</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>HWC / CCT</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Prog. Voltage</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Driver/Comparator</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Precision Clock</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Per-pin Voltage</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Per-pin Deskew</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Per-pin PMU</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Per-pin Load</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>System SMU</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

*6566 Only

<table>
<thead>
<tr>
<th>Interfacing</th>
<th>Characterization</th>
</tr>
</thead>
</table>

*6556 Only
### NI High Speed Digital Offering: Specifications

<table>
<thead>
<tr>
<th></th>
<th>6535/36/37</th>
<th>6541/42</th>
<th>6544/5</th>
<th>6551/52</th>
<th>6547/48</th>
<th>6555/56</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Form Factor</strong></td>
<td>PCIe / PXI</td>
<td>PCI / PXI</td>
<td>1 slot PXI</td>
<td>PCI / PXI</td>
<td>1 slot PXI</td>
<td>2 slot PXI</td>
</tr>
<tr>
<td><strong>Max Speed</strong></td>
<td>10/25/50 MHz</td>
<td>50/100 MHz</td>
<td>100/200MHz</td>
<td>50/100 MHz</td>
<td>100/200MHz</td>
<td>200 MHz</td>
</tr>
<tr>
<td><strong>Channels</strong></td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>20</td>
<td>32 / 24 (with HWC)</td>
<td>24</td>
</tr>
<tr>
<td><strong>Direction</strong></td>
<td>Input or Output</td>
<td>Input or Output</td>
<td>Bidirectional</td>
<td>In/Out or Bidirectional</td>
<td>Bidirectional</td>
<td></td>
</tr>
<tr>
<td><strong>Precision CLK</strong></td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Max DDR</strong></td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>400/300 Mbps (out/in)</td>
<td>No</td>
</tr>
<tr>
<td><strong>Voltage Levels</strong></td>
<td>Select 1.8, 2.5, 3.3, 5V*</td>
<td>Select 1.2, 1.5, 2.5, 1.8, 3.3 V</td>
<td>Program -2 to 5V (10 mV resolution)</td>
<td>Program -1.2 to 3.3V (100 mV resolution)</td>
<td>Program -2 to 7V (122 µV resolution)</td>
<td></td>
</tr>
<tr>
<td><strong>HWC/Tri-state</strong></td>
<td>No</td>
<td>No</td>
<td>Yes (20 ch)</td>
<td>Yes (24 ch)</td>
<td>Yes (24 ch)</td>
<td></td>
</tr>
<tr>
<td><strong>Streaming</strong></td>
<td>115 MB/s</td>
<td>400 / 660 MB/s</td>
<td>115 MB/s</td>
<td>400 / 660 MB/s</td>
<td>400 / 660 MB/s</td>
<td></td>
</tr>
</tbody>
</table>
PXle-6547/8 Digital Stimulus/Response Instruments

- 400 Mbps and 200 Mbps data rates with DDR
- 32 channels (24 with HWC)
- 1.2 – 3.3V (100mV steps)
- Onboard hardware compare with 6 logic states (1, 0, Z, L, H, X)
- 3 Banks of data delay for phase shifting data channels
- Onboard high resolution clock
## Digital ATE Logic States

<table>
<thead>
<tr>
<th>Logic States</th>
<th>Operation</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Drive States</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Drive logic low to DUT</td>
<td>• Stimulus response testing</td>
</tr>
<tr>
<td>1</td>
<td>Drive logic high to DUT</td>
<td>• Bit error rate testing (BERT)</td>
</tr>
<tr>
<td>Z</td>
<td>Tristate (high impedance)</td>
<td>• Manufacturing pass/fail tests</td>
</tr>
<tr>
<td><strong>Compare States</strong></td>
<td></td>
<td>• Failure analysis</td>
</tr>
<tr>
<td>L</td>
<td>Compare logic low from DUT</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>Compare logic high from DUT</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>Ignore the DUT output</td>
<td></td>
</tr>
</tbody>
</table>
HSDIO Features: Data Delay

- Available on all HSDIO modules

![Diagram showing data delay on different banks with respective percentages](image)

- Configurable on a **per-pin** basis on the PXIe-6555/6
- Configurable on a **per-bank** basis on the PXIe-6547/8
- Configurable on a **per-module** basis on all other products
HSDIO Features: Why Do We Need Tristate?

Tristate (Z) “turns off” the generation portion of a channel for that cycle.

Generate

Tristate

Acquire & Compare

1 0 0 1 0 1 Z Z H L L H L H

ni.com
HSDIO Features: Hardware Comparison

- Define / load expected values prior to running (H, L, & X)
- Acquired bits are compared against expected values in memory
- Errors show up in software API immediately
## Semiconductor Test: NI PXIe-6555/6

**Per-pin ATE Digital I/O**

<table>
<thead>
<tr>
<th>Specifications (per-pin)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O Data Rate</td>
<td>200 Mbps</td>
</tr>
<tr>
<td>Edge Placement</td>
<td>5 ns</td>
</tr>
<tr>
<td>Voltage</td>
<td>-2 to 7V (VOH, VOL, VIH, VIL, VTT)</td>
</tr>
<tr>
<td>PPMU Channels</td>
<td>24 data + 4 control</td>
</tr>
<tr>
<td>Current Ranges</td>
<td>2 uA to 32 mA with 1% accuracy</td>
</tr>
<tr>
<td>Implementation</td>
<td>PXIe, 2 Slots (700 MB/s streaming)</td>
</tr>
<tr>
<td>Deskew</td>
<td>30ps resolution per channel</td>
</tr>
</tbody>
</table>

**Advanced Features (6556 only)**

External SMU integration in place of PMUs, In-circuit calibration for production

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Active Load</td>
<td>24 mA</td>
</tr>
<tr>
<td>System TDR</td>
<td>Interconnect skew measurements into open load</td>
</tr>
</tbody>
</table>
NI PXIe-6555/6 – Voltage Features

Per Channel Voltage Control
-2V to 7V (-1V to 7V or -2V to 6V for generation)
- Programmable VOL, VOH, VTT, VIL and VIH

Voltage Threshold Testing
- Sweep voltages with 11 mV accuracy (122uV resolution).

Voltage High +7V
- DIO 0
- Voltage Low -2V

Voltage High +5V
- DIO 1
- Voltage Low 0V

ni.com
NI PXIe-6555/6 – Deskew Features

Per Pin Deskew with ~30ps resolution

- Set up and hold time measurements
- Delay measurements

200 MHz Clock

- Out
- In

DIO0
DIO1
DIO2
DIO3
...
**Per-Pin PMU (4 Quadrant)**

- Force and measure voltage and current

- Test 1 – Open/Shorts Testing
  - Parallel Test

- Test 2 – Current Leakage Tests
  - Parallel Test

- Test 3 – Digital Pattern I/O
  - Scripting for multiple patterns
What is “Edge Placement”? 

- Create an oversampled data set
  - At 100MHz we can have 10ns of edge placement resolution
  - Trade off timing resolution for memory depth
Timing Set Implementation

- Conversion of a WGL / STIL file to HWS
  - Partnership with TSSI
  - Convert industry standard to device specific waveforms
    - 200MHz product can mimic timing sets with 5ns of edge placement resolution
Electrical Test Today

Acquire, Transfer, Post-Process Paradigm

Fixed-Functionality
Triggers and Records

Open-Loop, Stimulus-Response Data

Test Vector and Waveform Synthesis and Analysis Tools
FPGA-Based Test Methods

Real-Time, Continuous Measurements

Custom Triggering and Acquisition

Closed-Loop and Dynamic Test

Protocol Emulation
FPGA Technology

Field-Programmable Gate Array

Programmable Interconnects

Logic Blocks

I/O Blocks

ni.com
Implementing Logic on an FPGA: $F = \{(A+B)CD\} \oplus E$
Why are FPGAs useful?

- **High Reliability** – Designs implemented in hardware
- **High Performance** – Computational abilities open new possibilities for measurement and data processing speed
- **True Parallelism** – Enables parallel tasks and pipelining, reducing test times
- **Low Latency** – Run algorithms at deterministic rates down to 5 ns
- **Reconfigurable** – Create DUT / application-specific personalities
A Simple Digital Protocol: I²C

Traditional Approach
- Static stimulus and expected responses
- Difficult to accommodate multiple clock domains
A Simple Digital Protocol: I²C

Protocol-Aware Approach
- Intelligence built into the tester
  - Accommodates wait cycles
  - Easy to cross clock domains
- Test with high-level commands
  - Real-world scenario
  - Inherently easier to program

Protocol-Aware Tester

Address, Data, Address, Receive

Integrated Circuit

SDA

SCL

Response Data
NI FlexRIO System Architecture

NI FlexRIO Adapter Module
- Interchangeable I/O
- Analog or digital
- NI FlexRIO Adapter Module Development Kit (MDK)

NI FlexRIO FPGA Module
- Virtex-5 FPGA
- 132 digital I/O lines
- Up to 512 MB of DRAM

PXI Platform
- Synchronization
- Clocking/triggers
- Power/cooling
- Data streaming

PXI/PXIe

ni.com
NI FlexRIO Architecture

- Synchronization
- Clocking/triggers
- Power/cooling
- Data streaming

NI FlexRIO Platform

- PXI/PXIe
- NI FlexRIO FPGA Module
- NI FlexRIO Adapter Module

- Virtex-5 FPGA
- 132 digital I/O lines
- Up to 512 MB of DRAM

- Interchangeable I/O
- Analog or digital
- NI FlexRIO Adapter Module Development Kit (MDK)

ni.com
NI FlexRIO HSDIO Adapter Modules

NI 6583 Mixed I/O FAM
• 19 LVDS channels, 200 MHz
• 35 single-ended channels, 200 MHz
• Selectable Voltage Levels (1.2, 1.5, 1.8, 2.5, 3.3 V)

<table>
<thead>
<tr>
<th>Product</th>
<th>Description</th>
<th>Platform</th>
<th>Channels</th>
<th>Maximum Rate (MHz)</th>
<th>Voltage Levels</th>
</tr>
</thead>
<tbody>
<tr>
<td>NI 6581</td>
<td>FPGA-based Digital I/O</td>
<td>PXI/PXIe</td>
<td>54</td>
<td>100</td>
<td>5.0, 3.3, 2.5, 1.8 V</td>
</tr>
<tr>
<td>NI 6583</td>
<td>FPGA-based Digital I/O</td>
<td>PXI/PXIe</td>
<td>19 / 35</td>
<td>200</td>
<td>LVDS, 1.2-3.3V</td>
</tr>
<tr>
<td>NI 6584</td>
<td>FPGA-based Digital I/O</td>
<td>PXI/PXIe</td>
<td>16</td>
<td>16 Mb/s</td>
<td>RS422/485</td>
</tr>
<tr>
<td>NI 6585</td>
<td>FPGA-based Digital I/O</td>
<td>PXI/PXIe</td>
<td>32</td>
<td>200 (300 Mb/s DDR)</td>
<td>LVDS</td>
</tr>
<tr>
<td>NI 6587</td>
<td>FPGA-based Digital I/O</td>
<td>PXI/PXIe</td>
<td>16</td>
<td>1Gbps</td>
<td>LVDS</td>
</tr>
</tbody>
</table>

ni.com
Questions